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Our Docket No.: 42390P9482

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Kumamoto et al.	Examiner:	Thai, Luan C.
Application No: 09/741,535	Art Unit:	2811
Filed: December 19, 2000		
For: Molded Flip Chip Package		

RESPONSE TO OFFICE ACTION

Box Non Fee Amendment
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action mailed December 17, 2001, the Applicant respectfully requests the Examiner to enter the following amendment and to consider the following remark.

FIRST CLASS CERTIFICATE OF MAILING

I hereby certify that I am causing the above-referenced correspondence to be deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and that this paper or fee has been addressed to the Assistant Commissioner for Patents, Washington, D. C. 20231

January 16, 2002
Date of Deposit

Krista Mathison
Name of Person Mailing Correspondence

Krista Mathison 1/16/02
Signature Date

AMENDMENTS

In the claims:

For the Examiner's convenience all pending claims are presented herein. Please amend the claims as follows:

1. A method comprising:

placing incomplete chip package into a mold, the incomplete chip package comprising a chip and a substrate electrically coupled using a flip chip process, the chip having (i) a top surface facing the substrate, (ii) a bottom surface opposite the top surface, and (iii) one or more side surfaces between the top and bottom surfaces;

injecting a liquid resin into mold, the resin encapsulating a significant portion of the one or more side surfaces, and filling a first gap between the top surface and the adjacent substrate; and

curing the resin.

2. The method of claim 1, wherein the chip and substrate were electrically coupled by a plurality of reflowed solder bumps.

3. The method of claim 1, wherein the incomplete chip package further comprises at least one passive component electrically coupled to the substrate.

4. The method of claim 1, wherein the resin comprises an epoxy.

5. The method of claim 4, wherein the resin further comprises a filler material.

6. The method of claim 5, wherein the filler material comprises silica spheres.

7. The method of claim 1, wherein the resin is injected under pressure.

8. The method of claim 1, wherein the resin encapsulates substantially all of the one or more side surfaces.

9. The method of claim 8, wherein the resin does not encapsulate the bottom surface.

10. The method of claim 1, wherein the mold comprises an upper mold cavity surface, and the bottom surface butts directly up against an adjacent portion of the upper mold cavity surface.

11. The method of claim 10, wherein a release film intervenes between the bottom surface and the upper mold cavity surface.

12. The method of claim 1, wherein the mold is maintained at an elevated temperature during said operation of injecting a liquid resin into the mold.

13. The method of claim 1, wherein the resin is cured by maintaining the resin at an elevated temperature for at least a predetermined period of time.

14. The method of claim 1, wherein the substrate is a thin substrate.

15. The method of claim 1, wherein the substrate is comprised of a polymeric material.

16. The method of claim 14, wherein the thin substrate is approximately 0.05mm to 0.5mm thick.

17. The method of claim 3, wherein said injecting a liquid resin into the mold also fills at a second gap between a first surface of the at least one passive component and an adjacent surface of the substrate.

18. The method of claim 3, wherein said injecting a liquid resin into the mold fully encapsulates the at least one passive component.

19. A flip chip package made according to the process of claim 1.

20. A method comprising:

placing an incomplete flip chip package into a bottom inner cavity of a bottom mold portion,

the incomplete flip chip package comprising a chip and a substrate, the chip having a top surface coupled by reflowed solder bumps to a upper surface of the substrate, the chip further comprising a bottom surface opposite the top surface and one or more side surfaces between the top and bottom surfaces;

mating an upper mold portion with the lower mold portion, the upper mold portion having an upper inner cavity, the upper and bottom inner cavities forming a mold inner cavity enclosing the incomplete flip chip package;

injecting a predetermined amount of a liquid resin into the mold inner cavity, the liquid resin encapsulating the substantially all of the one or more side surfaces and substantially all of the upper surface, the liquid resin further filling a gap between the top surface of the chip and an adjacent portion of the upper surface, encapsulating the reflowed solder bumps;

curing the liquid resin by maintaining the mold at an elevated temperature for a predetermined period of time, the elevated temperature being equal to or

greater than the cure temperature of the filled liquid resin for the predetermined period of time.

21. The method of claim 20, wherein the liquid resin comprises an epoxy and a silica filler.

22. The method of claim 20, wherein the substrate is a thin substrate having an approximate thickness of 0.05mm to 0.5mm.

23. The method of claim 20 further comprising:

removing the complete flip chip package from the mold inner cavity by separating the upper and bottom mold portions, the complete flip chip package comprising the incomplete flip chip package and the solidified filled resin adhesively bonded to the incomplete flip chip package.

24. A flip chip package produced using the process of claim 20.

25. The method of claim 20, wherein the bottom surface butts against an adjacent surface of the upper inner cavity.

26. The method of claim 25, wherein a release film intervenes between the bottom surface and the adjacent surface of the upper inner cavity.

Remarks

Applicant respectfully requests reconsideration of this application as amended. Claims 27-30 have been cancelled. Therefore, claims 1-26 are present for examination.

35 U.S.C. §121 Rejection

Elections/Restrictions

The Examiner, in the Office Action mailed December 17, 2001, has required under 35 U.S.C. 121 a restriction to one of the following inventions.

Group I: Claims 27-30 drawn to a semiconductor device, classified in class 257.

Group II: Claim 1- 26, drawn to a method of making a semiconductor device, classified in 438, subclass 106 +.

Accordingly, the Applicant elects, without traverse, Group II, (Claims 1-26) and requests that claims 27-30 be cancelled without prejudice. Therefore, claims 1-26 are present for examination.

Conclusion

Applicant respectfully submits that the claims as amended are now in condition for allowance. Accordingly, Applicant respectfully requests the claims as amended be allowed.

Invitation for a Telephone Interview

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Request for an Extension of Time

The Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17 for such an extension.

Charge our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date 1/16/02

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